LISTING OF THE CLAIMS

1. (Previously Presented) A method comprising:

issuing a load instruction to an execution cluster in an out of order processor;

allocating an entry for the load instruction in a structure for tracking only load instructions, if the load instruction utilizes speculative data; and

flagging a field in a reorder buffer to indicate the load instruction that uses speculative data is to be checked at retirement, the field in an entry tracking program order of the load instruction.

2. (Previously Presented) The method of claim 1, further comprising:

searching the structure to confirm the load data at the time of retirement.

3. (Original) The method of claim 1, further comprising:

invalidating the entry for the load instruction during a store instruction retirement if the store instruction conflicts with the load instruction.

4. (Original) The method of claim 2, further comprising:

flushing a pipeline if the structure for tracking only load instructions does not contain a valid entry for the load instruction at load instruction retirement.

5. (Original) The method of claim 1, wherein the load instruction is an advanced load instruction.

6. (Original) The method of claim 5, further comprising:

converting a basic load instruction into an advanced load instruction.

7. (Original) The method of claim 1, wherein the structure for tracking load instructions is an advanced load allocation table.

8. (Previously Presented) A device comprising:

a store queue in an out of order processor to track only store instructions;

a load queue coupled to the store queue to track only speculative load instructions; and

a reorder buffer to track program order of instructions, the reorder buffer including an entry to track program order of a load instruction, the entry including a field indicating the load instruction is to be checked at retirement.

9. (Previously Presented) The device of claim 8, further comprising:

an instruction scheduler coupled to the store queue to schedule instruction execution.

10. (Original) The device of claim 8, wherein the load queue is an advanced load allocation table.

11. (Previously Presented) A system comprising:

a first processor having at least a 64 bit architecture comprising a first data cache, a set of execution units, an out of order instruction scheduler coupled to the data cache and the set of execution units, a store queue coupled to the instruction scheduler to track only store instructions, a load queue coupled to the store queue to track only speculative load instructions, a reorder buffer to track program order of instructions, the reorder buffer including an entry to

track the program order of a load instruction, the entry including a field indicating the load instruction is to be checked at retirement;

a bus coupled to the processor; and

a system memory device coupled to the bus.

12. (Original) The system of claim 11 further comprising:

a second processor coupled to the bus comprising a second data cache.

13. (Canceled)

14. (Previously Presented) An apparatus comprising:

means for tracking only speculative load instructions; and

means for tracking all instructions in program order coupled to the means for tracking only speculative load instructions, comprising a field to indicate a load instruction is to be checked at retirement, the field in an entry tracking program order of the load instruction.

15. (Original) The apparatus of claim 14, further comprising:

means for tracking only store instructions coupled to means for tracking only speculative load instructions.

16. (Original) The apparatus of claim 14, further comprising:

means for flushing a pipeline upon detection that a speculative load is not present in the means for tracking only speculative loads at the time of load instruction retirement.

17. (Previously Presented) A machine readable medium having instructions stored therein which when executed cause a machine to perform a set of operations comprising:

tracking only a set of load instructions relying on speculative data in a first data structure of an out of order processor; and

tracking a set of instructions in program order in a second data structure having a field to indicate to check speculation in a load instruction at a time of load instruction retirement, the field in an entry tracking program order of the load instruction.

18. (Original) The machine readable medium of claim 17, having instructions stored therein which when executed causes a machine to perform a set of operations further comprising:

tracking only a set of store instructions in a store queue of the out of order processor.

19. (Original) The machine readable medium of claim 17, having instructions stored therein which when executed cause a machine to perform a set of operations further comprising:

invalidating allocated load instruction entries during store instruction retirement.

20. (Original) The machine readable medium of claim 17, wherein the first data structure is an advanced load allocation table.

21. (Original) The machine readable medium of claim 17, wherein the second data structure is a reorder buffer.

22. (New) A method comprising:

allocating a first entry for a load instruction in a reorder buffer, the first entry to track program order of the load instruction;

issuing the load instruction to an execution cluster in an out of order processor;

determining that it is unknown whether a memory address associated with a store instruction that is prior, in program order, to the load instruction conflicts with a memory address associated with the load instruction;

utilizing speculative data in an execution of the load instruction by the out of order processor, if it is determined that it is unknown whether the memory address associated with the store instruction conflicts with the memory address associated with the load instruction;

allocating a second entry for the load instruction in a load table, the load table being a structure for tracking only load instructions, the second entry including characteristics of an operation of the load instruction; and

flagging a field in the first entry in the reorder buffer, the field to indicate that the load instruction is to be checked in relation to the load table, to confirm accuracy of the speculative data used in the execution of the load instruction, at retirement of the load instruction.